Swiss Accelerator Research and Technology

CHART Scientific Report (Final Report for Phase 2)

Cryogenic Power Supply for Use in Cryo-Cooled HTS Magnet Systems (FCCee CPES)

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1. Introduction / Original goals of this project

Replacing low-temperature superconducting and/or normal conducting magnets by high-temperature superconducting (HTS) magnets could facilitate clearly improved energy efficiency of CERN's Future Circular Collider (FCC). Therefore, the FCCee HTS4 project investigates a full-scale HTS-magnet-based prototype of a short-straight section for the FCC-ee. Complementing this research, the FCCee CPES project targets a further reduction of the energy consumption by minimizing the heat leak-in into the HTS magnet's cryostat: Conventionally, the magnet power supplies are placed outside of the cryostat at room temperature and the high magnet currents require thick current leads into the cryostat as shown in **Fig. 1a**, resulting in significant heat leak-in and a correspondingly high power requirement for the cryocooler. Alternatively, a cryogenic power electronic supply (CPES), i.e., a step-down dc-dc converter, could be placed inside of the cryostat (see **Fig. 1b**) such that the current leads into the cryostat operate at a higher voltage level and hence with significantly lower currents (in particular, much lower than the magnet current), thereby reducing the heat leak-in.

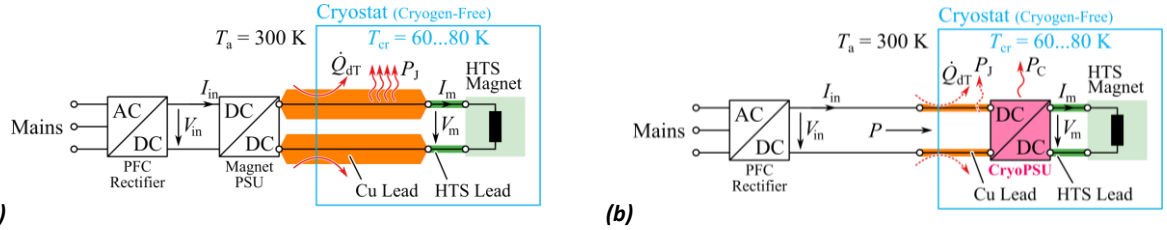

Fig. 1: (a) *Conventional HTS magnet power supply operating at room temperature; hence the current leads into the cryostat carry the full magnet current.* ***(b)*** *A cryogenic step-down dc-dc converter inside of the cryostat reduces the current levels in the current leads and hence the leak-in losses. The dc-dc converter developed in the FCCee CPES project generates about 5…6 W of heat load (including the residual leak-in losses) for the cryocooler at the rated magnet current of 250 A, which is an improvement of about a factor of four compared to the conventional solution from (a).*

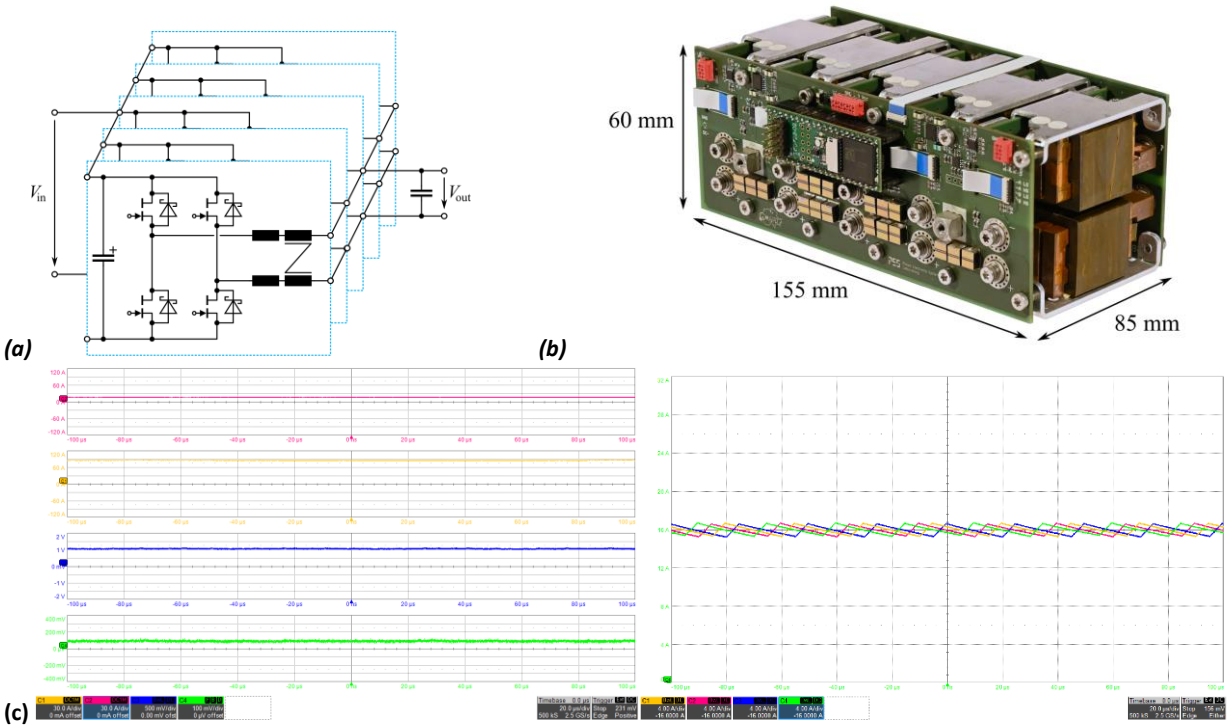

Fig. 2: (a) *Selected multiphase full-bridge topology with (exemplary) N = 5 phase modules (load-side EMI filter not shown).* ***(b)*** *GaN-based full-bridge phase module and* ***(c)*** *demonstrator system with N = 5 phase modules (total current rating of 80…100 A); the common-mode chokes (CMCs) and the EMI filter are not yet included.* ***(d)*** *Measured exemplary waveforms (RT) for operation with 1 V input and 40 mV output voltage and 85 A output current; note that only four out of five interleaved phase currents are shown due to limited channel count of the oscilloscope.*

The key challenge for the CPES lies in the ultra-low loss budget: To render the additional complexity of a cryogenic dc-dc converter worthwhile, an overall reduction of the cryocooler heat load to about 1/4 of the conventional solution (power supply at room temperature) is targeted. Specifically, considering the 250 A nominal current of the magnet designed in the scope of the FCCee HTS4 project, the conventional baseline solution results in a heat load of about 23 W with optimized current leads and a cryostat temperature of 60 K (first-stage); hence, the loss budget for the CPES, including the residual leak-in losses from the thinner current leads, is only 5…6 W.

The goal of the FCCee CPES project is thus to demonstrate the feasibility of a CPES for the FCCee HTS4 magnet with 250 A rated current, which achieves the targeted low losses, i.e., a reduced heat load of the cryocooler by a factor of about four compared to the state of the art.

2. Realisation

The basic functionality that the CPES must realize is that of a step-down (buck) dc-dc converter. Given the high output current of 250 A, paralleling of several power semiconductors is necessary to limit the conduction losses. However, instead of simply paralleling devices, it is beneficial to employ a so-called parallel-interleaved or multiphase buck converter, where the first switching-frequency harmonic that must be attenuated by the output filter appears at 2*N* times the device switching frequency (for *N* phase modules). Finally, to facilitate bipolar output voltage, e.g., to ramp down the magnet current at shut-down or, as detailed in the earlier reports, very quickly extract the magnet energy in case of quenching, a multiphase full-bridge topology as shown in **Fig. 2a** has been selected.

Further design considerations and optimizations have been described in [1] and a lossless method to balance the dc components of the phase currents in [2], preliminary results from component tests and

early prototype phase modules have been discussed in the earlier reports, and are not reiterated here. Thus, **Fig. 2b** shows the final CPES demonstrator with N = 5 phase modules for a target output current of about 80…100 A (due to the modularity of the selected approach, it has been decided that the feasibility of the loss budget etc. can be accurately and more expediently evaluated without a full-scale system). The dc input voltage is 1 V, which already results in very low input currents in the order of 5 A (compared to the magnet current of 250 A) due to the low power flow in steady state, i.e., essentially, only the losses of the CPES itself must be covered, as the HTS magnet is virtually lossless.

The phase modules employ four parallel GaN transistors (EPC2302) per switch position, which show a favourable reduction of the on-state resistance at cryogenic temperatures (specifically, about 800 µΩ per transistor at 77 K) compared to Si MOSFETs evaluated earlier. Similarly, for all types of electronic components (DSP/FPGA, ADCs, auxiliary power supplies/voltage regulators, gate drivers, current sensors, etc.) required by the CPES control hardware, suitable devices have been identified and tested in LN_2, whereby also the power consumption has been characterized to support an accurate estimate of the overall CPES losses.

Fig. 3a then shows first an estimation (calculation) of the loss breakdown of a phase module and measured losses of a single phase module operating in LN_2 and in a cryostat under vacuum at 77 K. A further measurement has been taken with interleaved operation of three phase modules with a combined dc output current of up to 80 A, confirming that the results from a single-module test can be used to assess the performance of a multi-module system very accurately.

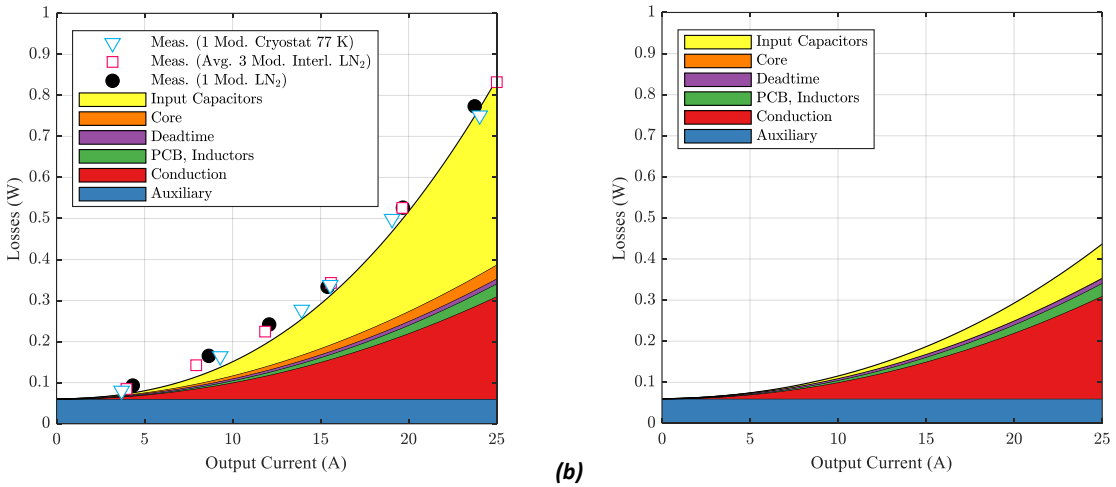

Fig. 3: (a) *Calculated and measured losses (at 77 K immersed in LN_2) of one and three modules with CMCs; the measured losses of the three-module setup have been scaled to one module (i.e., divided by 3) for comparison purposes. Due to measurement setup restrictions (precision shunt for load current measurement), a load resistance of 8 mΩ results, leading to relatively high duty cycles and high power flow. This causes high rms currents in the dc input capacitors and hence high losses due to their ESR.* ***(b)*** *Calculated loss breakdown assuming a (residual) load resistance of 0.8 mΩ, resulting in duty cycles and input capacitor losses that are closer to those expected in the final application with an HTS magnet load. Note further that, independent of the number of modules, a system-level loss contribution from the control electronics of about 1 W must be expected.*

Note further that an accurate electric measurement of the losses has been achieved using a shunt resistor in RT, resulting in a relatively high overall load resistance of about 8 mΩ. This, in turn, leads to operation with relatively high output voltage, thus high duty cycles, and relatively high high-frequency currents in the dc input capacitors. Especially at high output currents, these losses dominate. However, in the targeted application with an HTS magnet, the effective load resistance effectively consists only of the transistor on-state resistances and the resistances of the other CPES components (e.g., the inductors), and is thus at least an order of magnitude lower. As **Fig. 3b** shows, the input capacitor losses are

then expected to be much lower, further improving the overall performance. **Tab. 1** thus summarizes the expected losses of two different CPES realizations, using N = 12 or N = 15 phase modules, as N is a degree of freedom modifying the trade-off between realization effort/complexity and losses. Even when the losses as measured (i.e., considering high duty cycles that are not characteristic for the final HTS magnet application) are considered, a CPES-based solution would reduce the heat load to about 1/3 compared to the state of the art with an outside power supply at RT. If much lower output voltages / duty cycles are considered, i.e., as expected for the application with an HTS magnet load), a further reduction of the overall heat load to 4.4…4.8 W (for N = 15 or N = 12, respectively), or to around 20% of the state of the art, is expected. Note that the EMI filter components are not expected to significantly contribute to the losses, because the inductive components could be realized with HTS tape windings.

Tab. 1: *Expected losses for a 250-A CPES system for two different realizations with N = 12 and N = 15 phase modules. Note that the projections based on the available measurements are too pessimistic as in a final application with an HTS magnet load, much lower duty cycles and hence reduced input capacitor losses and inductor core losses are expected. The leak-in losses are estimated assuming optimized current leads (ratio of length to cross section).*

Phase count	Duty Cycle, *D*	Power stage (W)	Control (W)	Leak-in (W)	Total (W)	Rel. to Conv.*
12	as measured	6.7	1.1	0.7	8.5	37%
12	as exp. for HTS	3.3	1.1	0.4	4.8	21%
15	as measured	5.4	1.1	0.6	7.1	31%
15	as exp. for HTS	3.0	1.1	0.3	4.4	19%

* Conventional: Opt. 250-A current leads, first-stage cryostat temp. of 60 K, ambient temp. 300 K. => 23 W [1]

In the last few months of the project, an alternative phase module topology, the three-switch T-type (3S-TT) shown in **Fig. 4b**, has been identified [3]. The essential (functional) symmetry of GaN HEMTs indicated in **Fig. 4c** provides sufficient reverse blocking capability for the low dc input voltages (in the order of 1 V) of the CPES, and hence facilitates the realization of the T-type bridge-leg's midpoint switch with a single transistor (instead of an anti-series connection of two transistors conventionally used in T-type structures for higher dc voltages). Thus, in contrast to the full-bridge topology, always only *one* instead of two transistors is in the load current path reducing the transistor conduction losses by 50%.

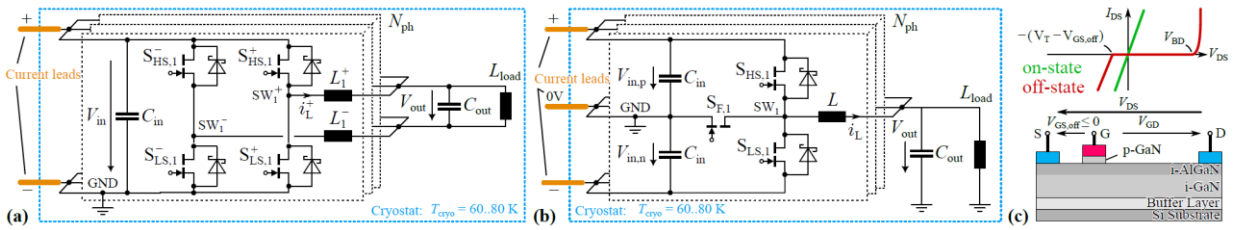

Fig. 4: ***(a)*** *Multi-phase full-bridge topology considered so far (CMCs not shown).* ***(b)*** *Multi-phase topology using the new three-switch T-Type (3S-TT) bridge-leg topology, where the midpoint switch SF,1 is realized with a single GaN transistor which, due to its inherent (functional) symmetry, features sufficient reverse voltage blocking capability for the low dc input voltages of around 1 V. Figure taken from [3], where further details are given.*

All other things being equal, i.e., same effective switching frequency at the output, same inductors, etc., the calculation results and the measurements presented in **Fig. 5** confirm the corresponding loss reduction achieved with a 3S-TT phase module compared to the FB phase module discussed earlier (note the correspondingly lower share of the conduction losses). As in the final application with an HTS load the transistor conduction losses dominate, the 3S-TT approach seems promising. On the other hand, 3 instead of only 2 input current leads are required; due to the lower losses (i.e., lower steady-state input power), these carry less current, however. More detailed evaluations are ongoing / in the scope of future work.

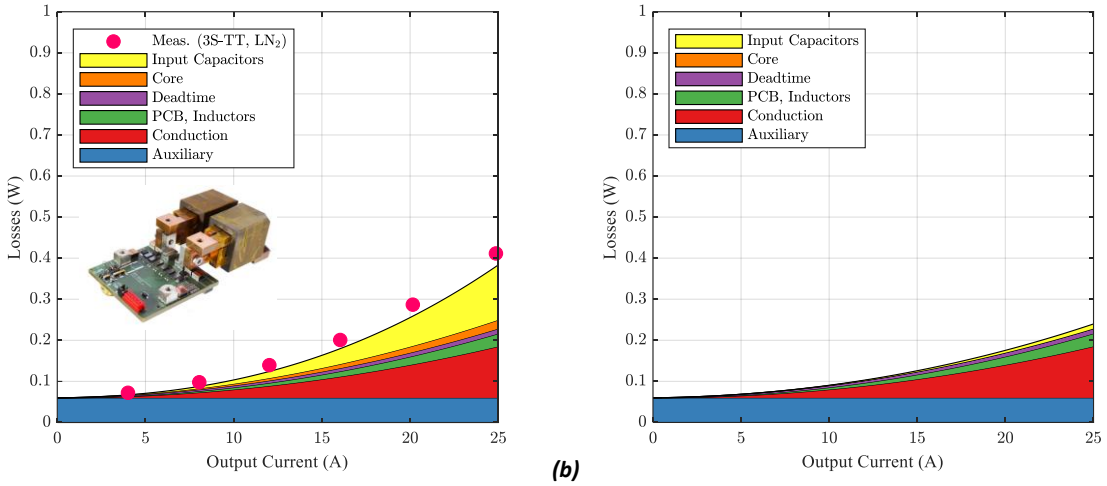

Fig. 5: (a) *Calculated and measured losses (at 77 K immersed in LN_2) of the 3S-TT phase module prototype (photo as an inset), using an effective load resistance of about 6 mΩ, leading to relatively high duty cycles and high power flow. This causes high rms currents in the dc input capacitors and hence high losses due to their ESR; however, note that the 3S-TT phase module prototype carries more parallel input capacitors than the FB phase module, hence their loss contribution is lower.* ***(b)*** *Calculated loss breakdown assuming a (residual) load resistance of 0.8 mΩ, resulting in duty cycles and input capacitor losses that are closer to those expected in the final application with an HTS magnet load. The expected loss savings of the 3S-TT over the FB module amounts to a halving of the conduction losses, i.e., to about 120 mW at 25 A.*

3. Results / Conclusions / Deliverables

In the scope of the FCCee CPES project, the feasibility of a cryogenic magnet power supply that facilitates about a fourfold reduction of the cryocooler heat load compared to the state of the art with power supplies operated outside of the cryostat at room temperature has been experimentally demonstrated. Even though the ultimate test with an actual HTS magnet load at PSI is still pending, much more extensive cryogenic testing than originally planned, both in LN_2 but also in a cryostat, have been conducted at ETHZ. Furthermore, a recently identified new bridge-leg topology (3S-TT) promises further loss reductions and/or lower realization effort. In principle, both approaches can be designed to integrate quench protection (i.e., fast energy extraction) functionality.

A key challenge for future work is reliability: During testing, in particular in LN_2 and correspondingly with quite fast temperature transients, we observed some component failures (e.g., of the employed acrylic film capacitors, or of some gate driver ICs). As no root-cause investigation has been carried out in the scope of the project, it is uncertain whether these failures are a consequence of the low temperature, the temperature transients, or the thermal cycles, or a combination of these factors. However, in any case when scaling up the CPES approach to the FCC-ee with its thousands of magnets and the need for very high availability, reliability and, given the modular architecture, redundancy aspects must be carefully studied. In principle, redundancy of phase modules could increase the availability almost arbitrarily in theory, the practical challenge consists of the need to identify and, in particular, isolate a faulty module form the rest of the converter *in a way that does not contribute to higher steady-state losses.* The 3S-TT phase module approach could be part of a solution, as then an additional switch could be placed in the output current path to disconnect a faulty module, while not exceeding the losses obtained with the baseline FB phase module.

A second vector for future research involves scaling up the CPES concept to much higher output current levels in the order of 10 kA, as required by the cryogen-free test station at PSI.

4. Publications and Outreach

The key project results have been published at three international conferences, and three journal publications are in preparation.

Published

[1] D. Cao, D. Zhang, J. W. Kolar, and J. Huber, "Conceptualization of a cryogenic 250-A power supply for high-temperature-superconducting (HTS) magnets of future particle accelerators," in *Proc. 11th Int. Conf. Power Electron (ICPE/ECCE Asia)*, Jeju, Korea, May 2023, pp. 688–696. doi: 10.23919/ICPE2023-ECCEAsia54778.2023.10213770.

[2] M. Akbas, D. Zhang, J. W. Kolar, and J. Huber, "New phase current balancing control for a cryogenic ultra-low-loss bidirectional multi-phase full-bridge DC-DC step-down converter," in *Proc. 10th IEEE Int. Power Electron. Motion Control. Conf. (IPEMC-ECCE Asia)*, Chengdu, China, May 2024, pp. 4921–4928. doi: 10.1109/IPEMC-ECCEAsia60879.2024.10567446.

[3] M. Akbas, J. W. Kolar, and J. Huber, "New cryogenic T-type three-switch low-voltage high-current 4Q power supply for HTS magnets," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE USA)*, Phoenix, AZ, USA, Nov. 2024.

In preparation

[a] D. Zhang, E. Bürgisser, M. Akbas, J. W. Kolar, and J. Huber, "A cryogenic 250-A power supply with < 5 W losses for high-temperature-superconducting (HTS) magnets of future particle accelerators," *IEEE Transactions,* in preparation.

[b] D. Zhang, M. Guerne-Kieferndorf, E. Bürgisser, M. Akbas, J. W. Kolar, and J. Huber, "Experimental evaluation of a new current balancing control method for a cryogenic ultra-low-loss multi-phase full-bridge DC-DC step-down converter," *IEEE Transactions,* in preparation.

[c] M. Akbas, D. Zhang, E. Bürgisser, J. W. Kolar, and J. Huber, "A new GaN T-type three-switch bridge-leg topology for cryogenic HTS magnet power supplies," *IEEE Transactions,* in preparation.

Note that titles are working titles only.

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