Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Zurich, February 06, 2024

CHART FCCee CPES

Cryogenic Power Supply for Use in Cryocooled HTS Magnet Systems

Yearly Report 2023

Dr. D. Zhang, E. Bürgisser, M. Akbas, Prof. Dr. J. W. Kolar, Dr. J. Huber
Power Electronic Systems Laboratory, ETH Zurich

Introduction

Replacing low-temperature superconducting and/or normal conducting magnets by high-temperature superconducting (HTS) magnets could contribute to the required energy efficiency improvement of CERN's Future Circular Collider (FCC-ee). Therefore, the FCCee HTS4 project investigates a full-scale HTS-magnet-based prototype of a short-straight section for the FCC-ee. Complementing this research, the FCCee CPES project discussed here targets a further reduction of the energy consumption by minimizing the heat leak-in into the HTS magnet's cryostat. This is achieved by placing a cryogenic power electronic supply (CPES), i.e., a step-down dc-dc converter, inside of the cryostat such that the current leads from the outside (room temperature) into the cryostat operate at a higher voltage level and hence significantly lower currents (in particular, much lower than the magnet current).

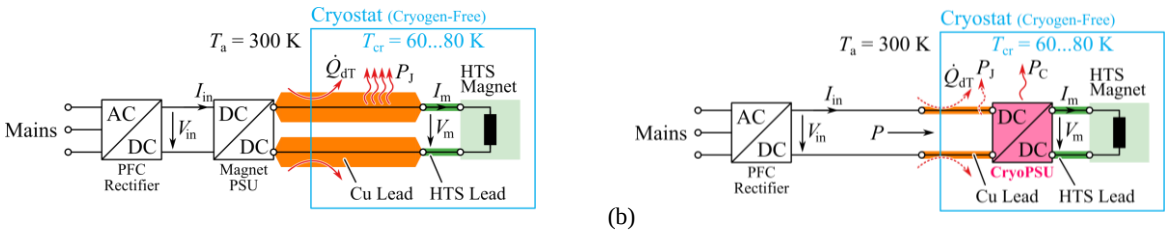

Fig. 1: (a) Conventional HTS magnet power supply operating at room temperature; hence the current leads into the cryostat carry the full magnet current. **(b)** A cryogenic step-down dc-dc converter inside of the cryostat reduces the current levels in the current leads and hence the leak-in losses. The dc-dc converter developed in the FCCee CPES project generates about 5…6 W of heat load (including the residual leak-in losses) for the cryocooler at the rated magnet current of 250 A, which is an improvement of about a factor of four compared to the conventional solution from (a).

The key challenge for the CPES lies in the ultra-low loss budget: to render the additional complexity of a cryogenic dc-dc converter worthwhile, an overall reduction of the cryocooler heat load to about 1/4 of the conventional solution (power supply at room temperature) is targeted. Specifically, considering the 250 A nominal current of the HTS4 magnet, the conventional baseline solution results in a heat load of about 23 W with optimized current leads and a cryostat temperature of 60 K (first-stage); hence, the loss budget for the CPES, including the residual leak-in losses from the thinner current leads, is only 5…6 W. **Fig. 1** visualizes the concept and **Fig. 2** shows the selected multiphase full-bridge dc-dc converter topology; these aspects and the conceptualization/optimization of the CPES have been described in the previous yearly report [1] and in a conference publication [2], and, for the sake of brevity, are not reiterated here.

In the course of 2023, the focus of the FCCee CPES project has then shifted from conceptualization and optimization to the hardware implementation, which is summarized below. Based on measurements of a representative phase module demonstrator, the CPES will meet the targeted loss budget, i.e., the cryocooler heat load can be reduced by a factor of four compared to the conventional solution.

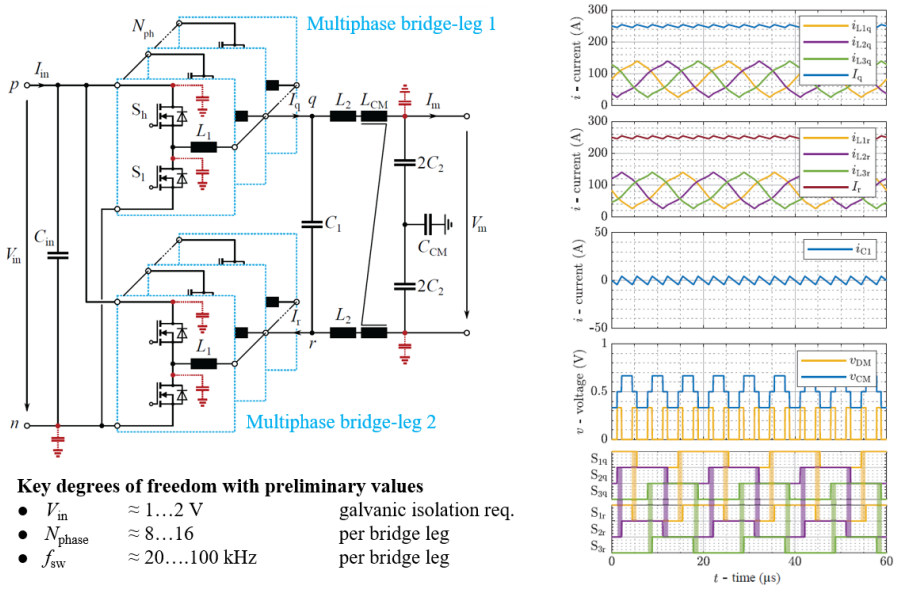

Fig. 2: Power circuit and key waveforms of the FCCee CPES interleaved multiphase full-bridge dc-dc step-down converter (for an exemplary N_{phase} = 3) from [2], which provides four-quadrant operation; for the rated output current of 250 A, 12…16 phase modules are needed.

Phase Current Balancing

Small mismatches in the equivalent dc resistances of the different phase modules, i.e., dominated by the on-state resistances of the transistors and the winding resistances of the phase inductors, result in unequal sharing of the magnet dc current among the phase modules and hence adversely

impacts the (dominant) conduction losses. Therefore, the phase current balancing must be actively controlled. Typically, e.g., in CPU power supplies where similar topologies are used, the phase currents are sensed by means of shunt resistors or the dc resistances of the phase inductors. However, given the tight loss budget of the CPES, these approaches are not feasible. Therefore, a phase current reconstruction method that relies on comparably straightforward and essentially lossless measurements of the input dc voltage has been developed and will be discussed in detail in [3].

Phase Module Demonstrators

Given the modular structure of the CPES topology shown in **Fig. 2**, initial testing has been carried out considering a single full-bridge phase module.

Si and GaN Transistors

To minimize the transistor conduction losses and at the same time limit the number of parallel transistors per switch position, devices with the lowest on-state resistances, $R_{ds,on}$, available in a single package are considered. Candidate devices are a 0.29 mΩ, 25 V Si MOSFET and a 1.8 mΩ, 100 V GaN HEMT (both resistances are nominal values at room temperatures). **Fig. 3** shows measured on-state resistance characteristics for different temperatures between room temperature and the 77 K of LN_2. It turns out that the low-voltage Si MOSFET starts to suffer from carrier freezeout already at around 100 K; this effect has been measured for various other low-voltage Si MOSFETs (not shown here), making LV Si technology not suitable for the CPES; in particular, since ultimately operation at lower temperatures than 77 K should be possible, too.

In contrast, the 100 V GaN transistor performs favorably, with a significant reduction of the on-state resistance at 77 K compared to room temperature. On the other hand, parallel-connection of four devices will be necessary to achieve similarly low on-state resistance as a single Si transistor.

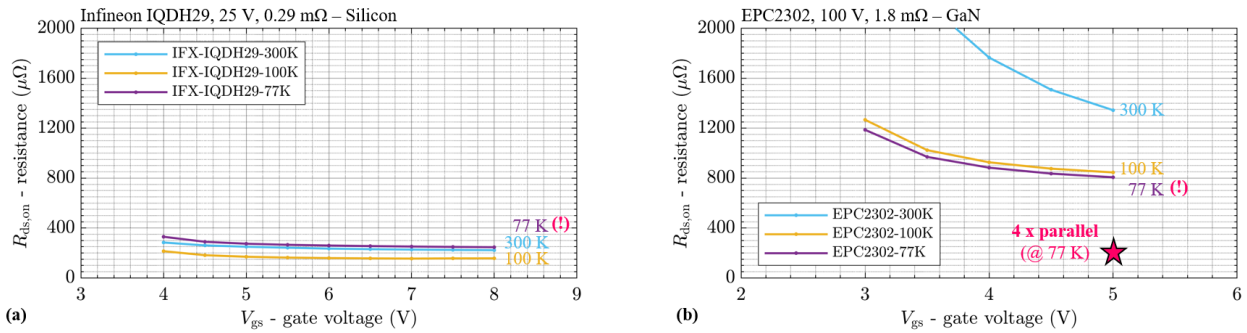

Fig. 3: Measured on-state resistances at different temperatures of **(a)** 25 V Si MOSFETs and **(b)** 100 V GaN HEMTS. Si MOSFETs offer lowest on-state resistance per single package, but due to carrier freezeout effects (in particular for low-voltage devices) perform badly at cryogenic temperatures. On the other hand, GaN HEMTs show a clear reduction of the on-state resistance for decreasing temperatures.

The 100 V blocking voltage rating of the GaN transistors is much higher than the CPES dc input voltage of around 1 V (yet still the best selection considering minimum on-state resistance per single package). Advantageously, the blocking voltage reserve could be utilized to implement the energy extraction capability necessary for quench protection of the magnet directly in the CPES as shown in **Fig. 4**

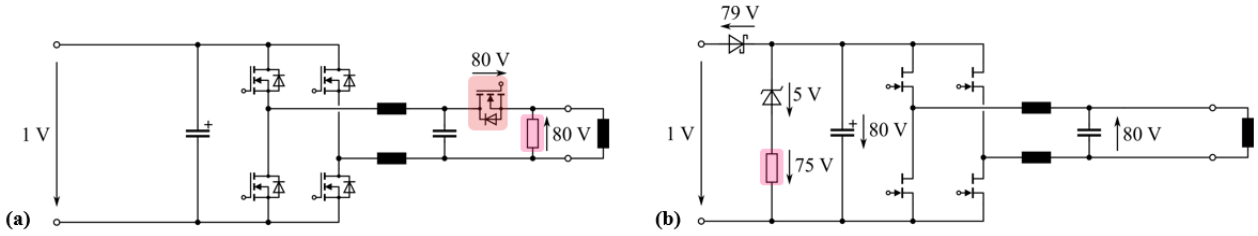

Fig. 4: Energy extraction for magnet protection, which requires a negative voltage of about 80 V across the magnet (based on preliminary HTS4 data). **(a)** A CPES with 25 V Si transistors would require a series switch with about 100 V blocking capability, which adds to the conduction losses. **(b)** The selected 100 V GaN-based CPES can be utilized to extract the magnet energy and possibly even transfer it out of the cryostat to an external dump resistor. Note that for the sake of clarity, only single full bridges and not the entire multiphase structures are shown.

GaN-Based Phase Module

To verify the loss estimates from the optimization phase, a GaN-based phase module demonstrator has been designed, commissioned, and characterized in LN_2, see **Fig. 5**. The measured power-stage losses for different dc output currents and two switching frequencies are shown in **Fig. 6a**, and **Fig. 6b** shows the projected losses for a multiphase system with different numbers of phase modules. The experimental results obtained with a single phase module suggest power-stage losses of 3.8 W to 4.4 W (for designs with 16 and 12 phase modules, respectively), which leaves some margin for the auxiliary electronics and residual leak-in losses.

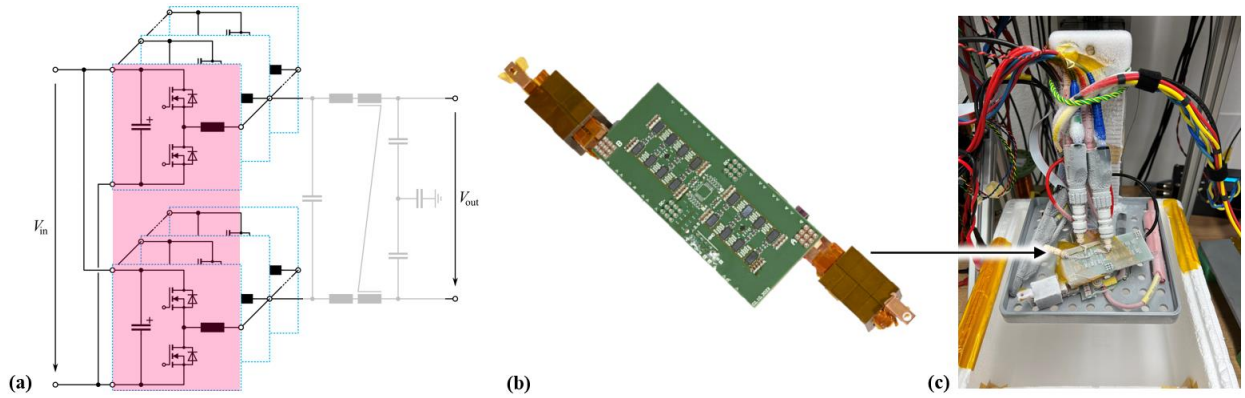

Fig. 5: Phase module demonstrator with 1.8 mΩ, 100 V GaN transistors (EP2302). **(a)** Power circuit, **(b)** photo of the phase module, where the four parallel devices per switch position and the two phase inductors are clearly visible, and **(c)** photo of the test setup just after elevating the device under test (the phase module) out of the LN_2.

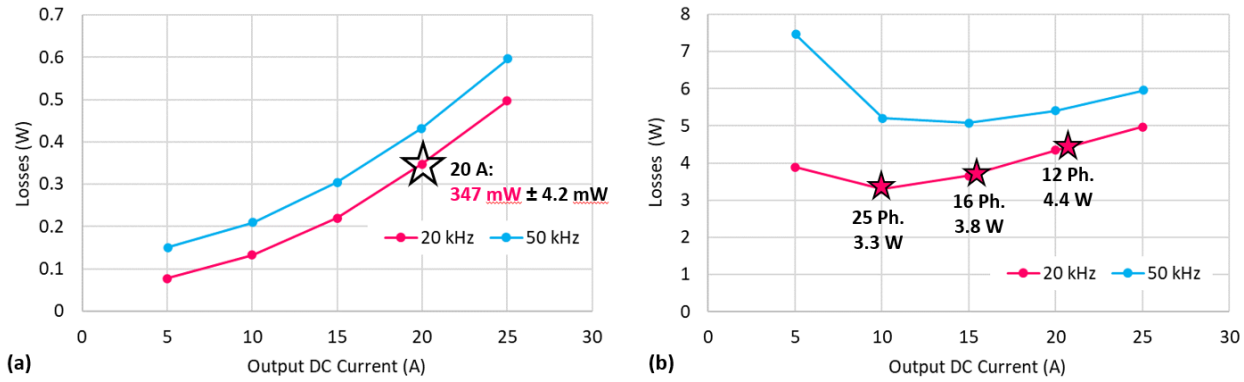

Fig. 6: (a) Measured power-stage losses of the GaN-based phase module operating immersed in LN_2 at 77 K at two different switching frequencies. **(b)** Projected overall power-stage losses at the rated output current of 250 A for different number of phase modules.

Control and Auxiliary Electronics

For all types of electronic components (DSP/FPGA, ADCs, auxiliary power supplies/voltage regulators, gate drivers, current sensors, etc.) required by the CPES control hardware, suitable devices have been identified and tested in LN_2, whereby also the power consumption has been characterized to support an accurate estimate of the full CPES losses.

Overall CPES Loss Projection

Based on measured losses of the power stage (one phase module) and the measured power consumption of the auxiliary electronics, the overall heat load generated by two different 250-A CPES configurations (different number of phase modules) with 20 kHz switching frequency can be estimated:

Phase count	Power stage (W)	Control (W)	Leak-in (W)	Total (W)	Rel. to Conv.*
12	4.4	1.1	0.5(5)	6.0	26%
16	3.7	1.1	0.5(2)	5.3	23%

* Conventional: Opt. 250-A current leads, first-stage cryostat temp. of 60 K, ambient temp. 300 K. => 23 W [1]

These projections indicate that the CPES will meet the challenging loss budget and hence reduce the overall heat load to the cryocoolers to about 25% of the conventional solution (room-temperature power supply).

Outlook

The design phase of the final CPES demonstrator has started and **Fig. 7** shows preliminary renderings of the final phase module design and the assembly of an 8-module unit; the 250-A CPES consists of two such units.

To limit testing time, the verification tests will employ lower but representative number of phase modules, e.g., four or five. Initial testing will be carried out at ETHZ using LN_2, where a special focus is on the experimental verification of the proposed phase-current sharing method [3]. Final tests will then be carried out in a cryostat at PSI.

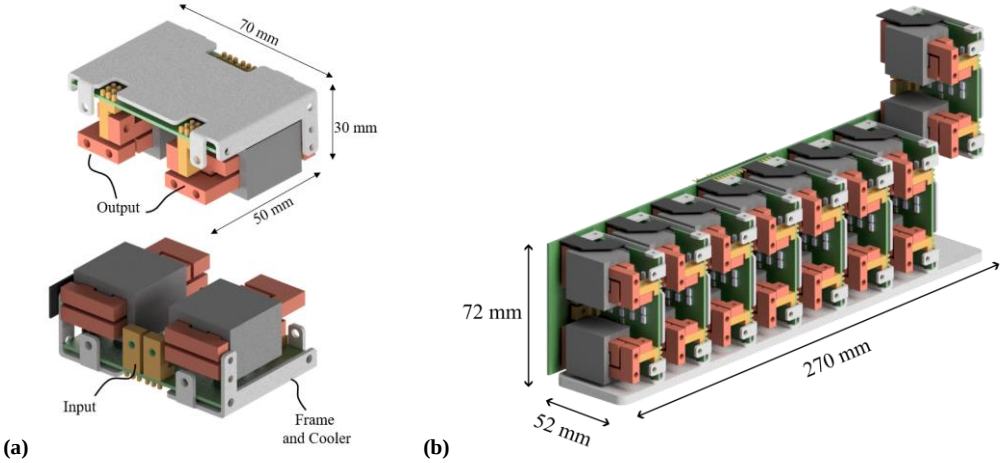

Fig. 7: 3D CAD rendering of the CPES prototype system currently under development. **(a)** Phase module and **(b)** converter with eight phase modules (two such blocks with a total of 2 x 8 = 16 phases form the full 250-A CPES).

References / Publications

[1] CHART FCCee CPES, “Cryogenic power supply for use in cryocooled HTS magnet systems -- Yearly Report.” 2022. [Online]. Available: https://chart.ch/wp-content/uploads/2023/02/FCCee-CPES-2022.pdf

[2] D. Cao, D. Zhang, J. W. Kolar, and J. Huber, “Conceptualization of a cryogenic 250-A power supply for high-temperature-superconducting (HTS) magnets of future particle accelerators,” in *Proc. 11th Int. Conf. Power Electron. (ICPE/ECCE Asia)*, Jeju, Korea, May 2023, pp. 688–696. doi: 10.23919/ICPE2023-ECCEAsia54778.2023.10213770

[3] M. Akbas, E. Bürgisser, D. Zhang, J. W. Kolar, and J. Huber, “New phase current balancing control for a cryogenic ultra-low-loss bidirectional/bipolar multi-phase DC-DC step-down converter,” in *Proc. 10th Int. Power Electron. Motion Contr. Conf. (IPEMC/ECCE Asia)*, Chengdu, China, May 2024, accepted for publication.