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CHART FCCee CPES
Cryogenic Power Supply for Use in Cryocooled HTS Magnet Systems

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D. Cao, D. Zhang, Prof. Dr. J. W. Kolar, Dr. J. Huber
Power Electronic Systems Laboratory, ETH Zurich

Introduction

The CERN Future Circular Collider (FCC-ee) feasibility study aims, amongst other advancements, at improved energy efficiency. Normal-conducting magnet systems with excessively high power consumption should thus be replaced by high-temperature superconducting (HTS) systems. This is investigated by the FCCee HTS4 project, which targets a full-scale HTS-based prototype of a short-straight section for the FCC-ee[1]. A further reduction of the energy consumption can be achieved by minimizing the heat load of the cryocoolers, which typically consume 20 W for each 1 W to be extracted from a cryostat at T_{cr} = 60 K against an ambient temperature of T_a = 300 K [1].

Conventionally, power converters that supply cryo-cooled HTS magnets with the necessary high DC currents of high quality (ripple, stability, etc.) are placed outside of the cryostat [2]–[4], and hence the high magnet current flows also in the current leads that penetrate the cryostat wall as shown in **Fig. 1a**. The copper current leads must therefore be of sufficiently large cross section. The thus formed thermal leakage path together with Joule heating results in a certain heat flow into the cryostat. For the considered case with a nominal magnet current of $I_{m,n}$ = 250 A, the heat leak-in amounts to about 23 W (again for T_{cr} = 60 K and T_a = 300 K).

Obviously, increasing the voltage level at which the power transfer into the cryostat takes place enables to design the current leads for a correspondingly lower current. Whereas this reduces the heat leak-in, a cryogenic power converter that ultimately provides the high DC currents to the HTS magnet is needed, see **Fig. 1b**. As this converter resides *inside* of the cryostat, it must operate at cryogenic temperatures of about 60…80 K, and its losses must be limited to low values (i.e., for the given case to < 0.5 · 23 W ≈ 12 W) such that a clear reduction of the cryocooler power rating can be achieved (note, however, that the cooling of the power electronics nevertheless poses a

[1] https://cerncourier.com/a/fcc-ee-designers-turn-up-the-heat/

challenge due to the vacuum environment). Such smaller cryocoolers could ultimately facilitate even wall-pluggable, standalone (i.e., without the need for cooling water supply, etc.) HTS magnet systems, e.g., for off-site medical or research applications. Thus, since August 2022, the FCCee CPES project investigates the feasibility of such a cryogenic power electronic supply (CPES) system for HTS magnets.

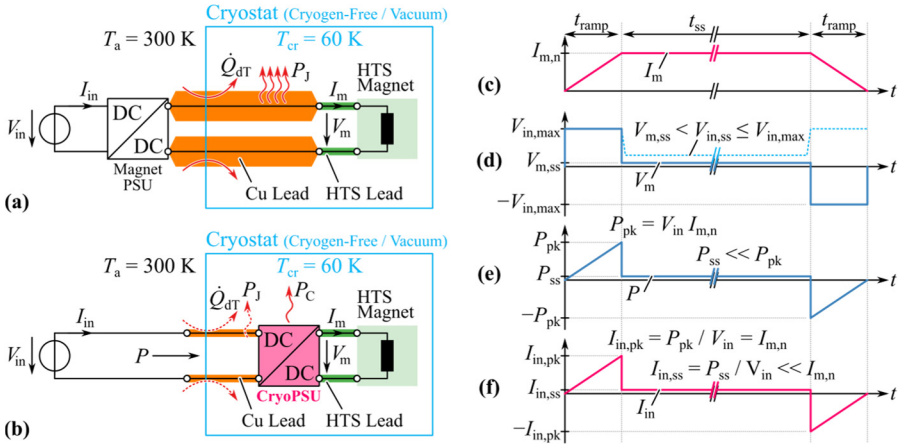


Fig. 1: (a) Conventional magnet power supply, where the magnet current, I_m, defines the required cross section of the feedthroughs from the warm environment into the cryostat chamber. **(b)** Proposed cryogenic magnet power supply, where a DC-DC step-down converter operating inside of the cryostat decouples the feedthrough current from the magnet current. **(c)** Typical mission profile for particle accelerator applications, where after a quick ramp-up phase, the magnet current is kept at a constant DC value for many hours before being ramped down again (note that both voltage polarities are needed to do so). **(d)** shows the required magnet voltage, V_m, which in steady-state is near-zero (very low resistive components / losses), and the adaptive (externally) input voltage V_{in}; **(e)** and **(f)** indicate the resulting input power and the input current. Note that the input current is near-zero in steady-state operation.

Summary of Activities

Literature Review on Cryogenic Power Electronics

A power electronic converter system consists of a multitude of different components such as power semiconductors of various types, magnetic components, capacitors, control electronics, etc. Typically, manufacturers specify components only for temperatures above −40 °C (233 K). To establish an initial understanding of what components can potentially be employed at the 60 K level, a literature review has been carried out. Whereas the results were encouraging (there is quite some interest in cryogenic power electronics, mainly targeting future aircraft applications where liquid-nitrogen-immersed systems could facilitate higher efficiencies and more compact realizations), they also indicate the need for careful testing of all components needed in candidate topologies. This is especially so because the CPES will not only operate at cryogenic temperatures but also under vacuum, which complicates cooling and rules out certain component technologies (as there should be no voids / air bubbles inside of a component). However, in contrast to the original project plan, we have decided to reorder the next steps, i.e., with the general component availability clarified by the literature review, it seemed more opportune to first investigate and decide on a suitable topology and then start with cryogenic prequalification tests of those components actually needed.

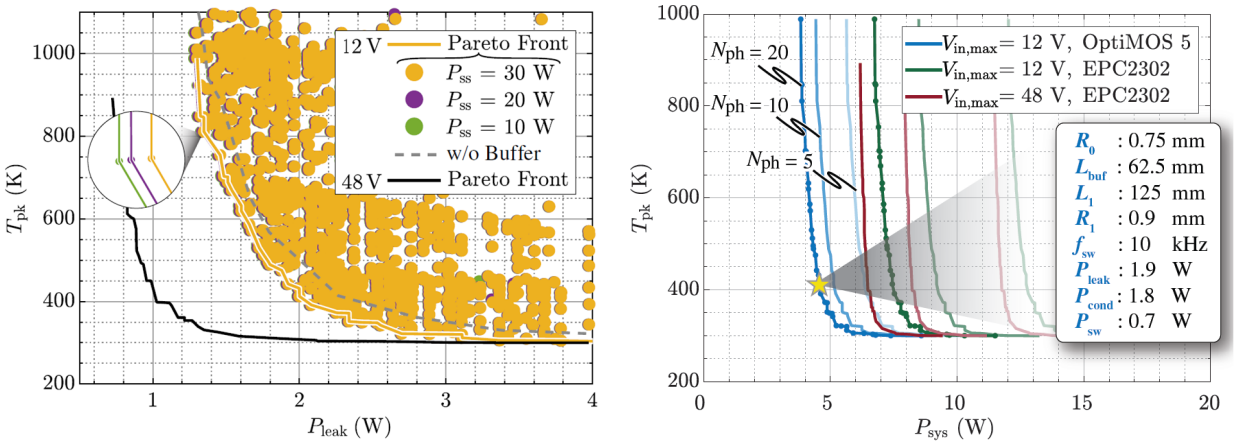
System-Level Considerations

As can be seen in **Fig. 1c-f**, a typical operation cycle of a HTS magnet in an accelerator applications features two distinct phases: (1) During a ramp-up phase the magnet is energized within typically less than 1000 s. Note that the ramp-down phase is equivalent to the ramp-up phase but with reverse power flow, which implies that the CPES must allow bidirectional power flow and thus feature a bipolar output voltage. (2) Then, there is a steady-state phase where the magnet current is roughly constant for many hours. Clearly, the steady-state input power is significantly lower (and, for the given case, essentially limited to the 12 W mentioned above) than the input power required during the ramping phases, where, in addition to supplying the converter and magnet losses, also the energy content of the magnet must be changed.

There are tow basic options to handle this increased power flow during the ramping phases:

1. Increasing the input voltage and keeping the input current constant allows to design optimal current leads for the steady state, but possibly requires a higher voltage rating of the CPES' power semiconductors, which typically implies worse performance (e.g., higher switching losses) that also affects the steady-state converter losses. Furthermore, a higher input voltage impacts the design of the EMI filter components, etc.
2. Increasing the input current and keeping the input voltage constant avoids these drawbacks, but on the other hand implies that current leads which are thicker than the steady-state optimum size must be used. This results in increased heat leak-in also in the steady state.

Of course, hybrid options do exist, too, i.e., the input voltage could be increased only slightly during the ramping phases, etc.



(a) **(b)**

Fig. 2: (a) Trade-off between the transient peak temperature, T_{pk}, in the current leads and the steady-state leak-in power, P_{leak}, which is rather independent of the steady-state power transfer, P_{ss}, into the cryostat. **(b)** Trade-off between T_{pk} and the *sum* of the leak-in power and the converter losses (P_{sys}), considering different maximum input voltages and hence different semiconductor technologies. Note: numerical results are preliminary; details will be given in [5].

It is interesting to consider a very short ramp time of only a few seconds[2], because then the heat capacity of a current lead designed for the low steady-state current could be leveraged to limit the lead's temperature rise caused by the higher current during the ramping phase. As shown in

[2] Note that such fast rates of rise of the magnet current are not needed in the FCC-ee application and might even be problematic as there is a risk of eddy current formation in the HTS magnets.

Fig. 2a there is a trade-off between the transient peak temperature of the leads and the steady-state thermal leak-in power. The trade-off favors higher input voltages during the ramping phase, which is then shorter and hence the smaller heat capacity of a thinner lead is sufficient to limit the peak temperature. Without going into details (these will be described, amongst other details, in an upcoming conference paper, see “Publications”), a holistic view must also include the power converter: considering an exemplary multiphase-buck dc-dc converter (see below), **Fig. 2b** shows that if the converter steady-state losses are considered, too, (instead of only the leak-in losses), a lower maximum input voltage gives the most favorable trade-off. Therefore, aiming at an optimum CPES, we must shift the system boundaries to include not only the power converter but also the current leads in the design considerations.

Topology Selection for First Demonstrator

In general, various isolated and non-isolated converter topologies could be considered. However, it seems reasonable to, first, limit the functionality of the cryogenic power converter to those aspects that are strictly needed at the interface to the magnet. Secondary features such as galvanic isolation and/or an initial step-down to a suitable, possibly variable, DC input voltage, etc. can be implemented *outside* of the cryostat if needed. Note also that this is sensible from an efficiency point of view because each watt of losses dissipated *inside* of the cryostat leads to a 20 W increase of the overall system losses via the cryocooler; this penalty does not apply to losses of converter stages that are outside of the cryostat.

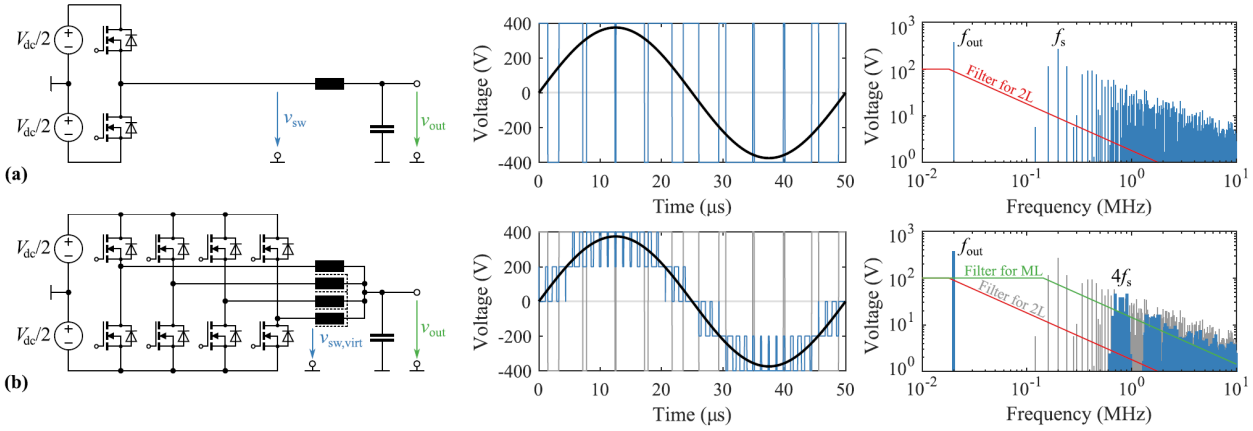


Fig. 3: (a) Single half-bridge with LC output filter and **(b)** multiphase buck topology with $N = 4$ half-bridges that operate in an interleaved manner and hence advantageously allow for a n increased filter cutoff frequency for a given noise criteria (image from [6]).

Thus, the basic functionality that the cryogenic power converter must realize is that of a step-down (buck) dc-dc converter. Given the high output current of 250 A, paralleling of several power semiconductors is necessary to limit the conduction losses such that the tight loss budget (12 W) can be met. In addition to this requirement of very low losses, further challenges include a high output voltage control bandwidth (in the order of about 1…10 kHz, to provide sufficient margin for an outer magnet current control loop) and, in particular, the electromagnetic compatibility (EMC) requirements in the CERN environment, i.e., an output voltage with very low high-frequency noise is needed to prevent any negative effect on, ultimately, the beam quality. The latter two aspects are similar to requirements for high-bandwidth digital power amplifiers. As shown in **Fig. 3**, instead of simply paralleling devices (i.e., realizing each of the transistors shown in **Fig. 3a** with several

physical devices connected in parallel), it is beneficial to employ a so-called parallel-interleaved or multiphase buck converter, see **Fig. 3b**. Advantageously, under ideal conditions the first switching-frequency harmonics appear around an *effective* switching frequency that is *N* times (for *N* phases) higher than the switching frequency of a given bridge-leg. Thus, to maintain a certain output voltage ripple, a correspondingly higher filter cutoff frequency suffices, which translates into smaller and/or less lossy EMI filter components. Alternatively, a lower device switching frequency and hence lower switching losses could be selected.

Finally, as the output voltage is, in steady state, very small and, because of the ramp-up/down phases, must be bipolar, we finally consider a full-bridge arrangement as shown in **Fig. 4** for the first demonstrator system. This ensures best utilization of the available input voltage (as compared to a half-bridge shown in the previous figure) and, advantageously, by allowing to operate each bridge-leg at a duty cycle of around 0.5 even for near-zero output voltages, achieves similar losses in all power semiconductors.

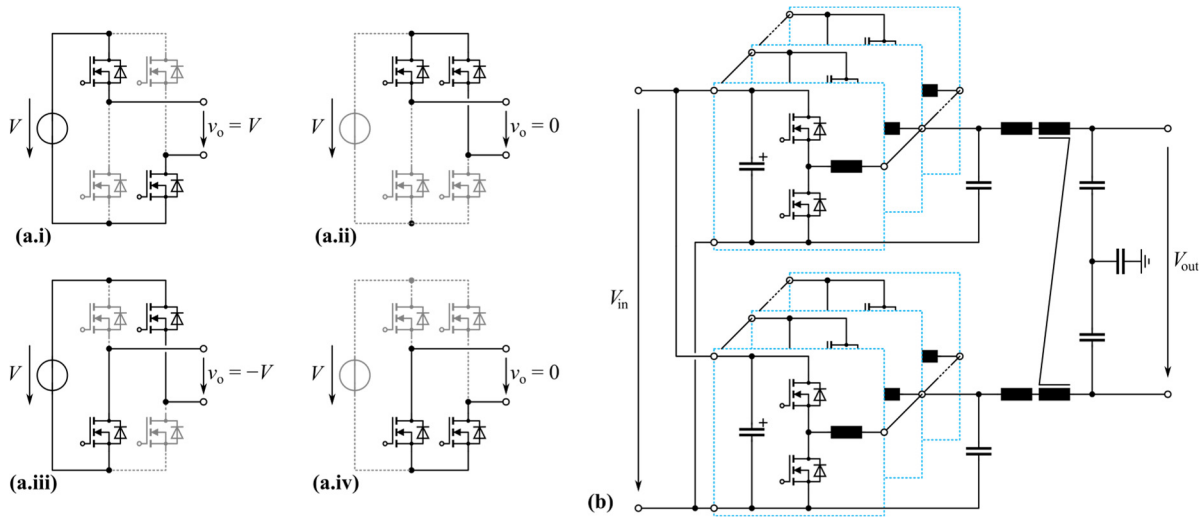


Fig. 4: (a) Switching states of a full bridge; note that the output voltage can be of both polarities. **(b)** Main power circuit of the first demonstrator featuring bipolar output voltage (full-bridge realization, each “bridge-leg” consists of several, for the first setup eight, parallel-interleaved half-bridges using 25 V, 0.5 mΩ silicon MOSFETs). Note that the input voltage, V_{in}, might be variable (using a dedicated converter stage outside of the cryostat) and that the passive damping elements of the EMI filter, sensors, control electronics, etc. are not shown.

Conclusion and Outlook

Currently, the detailed design of a dc-dc converter based on the topology shown in **Fig. 4** is well underway, also considering the system-level aspects mentioned earlier. Preliminary results indicate that the loss budget can be met using an input voltage (in steady state) of about V_{in} = 1 V and N = 8 phases per half-bridge realized with 25 V, 0.5 mΩ (300 K) silicon MOSFETs.

Thus, test PCBs for component tests (MOSFETs, current sensors, etc.) are being designed and initial tests, first in a warm environment to verify the MOSFET’s switching behavior at unusually low voltages, and ultimately at cryogenic temperatures in liquid nitrogen, are planned for Q1/23.

In parallel, a full prototype converter will be designed and commissioned, partly in the scope of an MSc thesis project that starts in 02/23. We expect a first working prototype to be ready in Q3/23, i.e., according to the project plan (milestone M3).

Team

The following table gives an overview on the project team members:

Danqing Cao	Scientific Assistant	08/22 – 12/22	100%	CHART
Daifei Zhang	PhD Student	08/22 – 12/22	10%	ETH
Dr. Jonas Huber	Senior Researcher	08/22 – 12/22	n/a	ETH
Prof. Dr. Johann W. Kolar	Professor	08/22 – 12/22	n/a	ETH

Publications

- D. Cao, D. Zhang, J. W. Kolar, and J. Huber, “Multi-objective optimization of cryogenic power supply for high-temperature-superconducting (HTS) magnets of future particle accelerators,” under review for publication at the *11th Int. Conf. Power Electron. (ICPE/ECCE Asia),* Jeju, South Korea, May 2023.

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